HD44105

(Dot Matrix Liquid Crystal Graphic Display Common Driver)

Description

The HD44105H is a common signal driver for LCD dot matrix graphic display systems. It generates the timing signals required for display with its internal oscillator and supplies them to the column driver (HD44102H) to control display, also automatically scanning the common signals of the liquid crystal according to the display duty cycle.
It can select 7 types of display duty cycle 1/8, 1/12, 1/16, 1/24,1/32, 1/48, and 1/64. It provides 32 driver output lines and the impedance is low (1 kΩ max) enough to drive a large screen.

Features

- Dot matrix graphic display common driver including the timing generation circuit
- Internal oscillator (Oscillation frequency is selectable by attaching an oscillation resistor and an oscillation capacitor)
- Generates display timing signals
- 32-bit bidirectional shift register for generating common signals
- 32 liquid crystal driver circuits with low impedance
- Selectable display duty ratio: 1/8, 1/12, 1/16, 1/24, 1/32, 1/48, 1/64
- Low power dissipation
- Power supplies: V_{CC} = +5 V ± 10%
  V_{EE} = 0 to –5.5 V
- CMOS process

Ordering Information

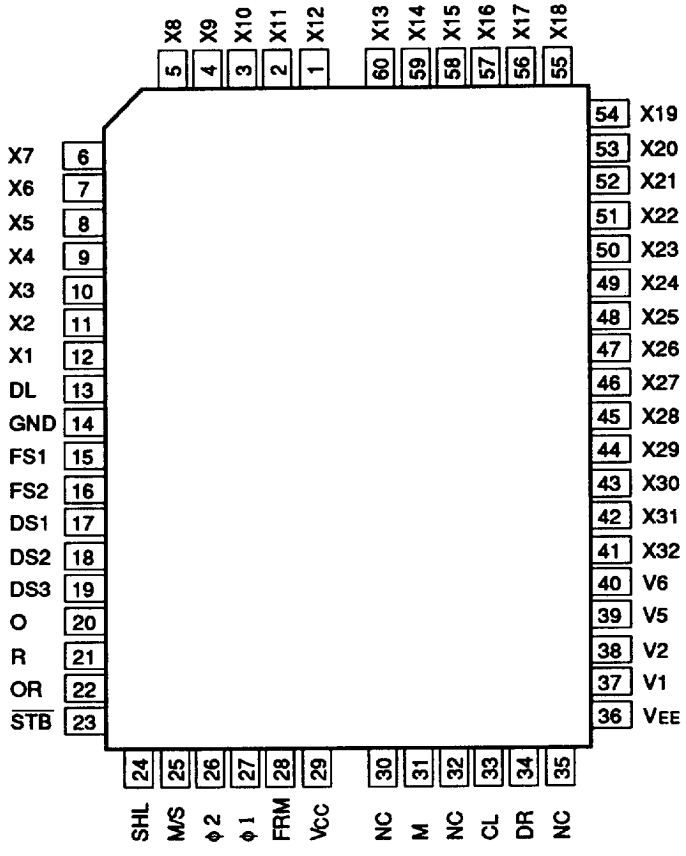
Type No.	Package
HD44105H	60-pin plastic QFP(FP-60)
HD44105D	Chip

Absolute Maximum Rating (Ta =25°C)

Item	Symbol	Ratings	Unit	Note
Supply voltage (1)	V_{CC}	–0.3 to +7.0	V	1
Supply voltage (2)	V_{EE}	V_{CC} –13.5 to V_{CC} +0.3	V	
Terminal voltage (1)	V_{T1}	–0.3 to V_{CC} +0.3	V	1, 2
Terminal voltage (2)	V_{T2}	V_{EE} –0.3 to V_{CC} +0.3	V	3
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +125	°C	

Notes: 1. Referred to GND = 0 V.
2. Applied to input terminals (except for V1, V2, V5, and V6) and I/O common terminals.
3. Applied to terminals V1, V2, V5, and V6. Connect a protection resistor of 47 Ω ± 10% to each terminal in series.

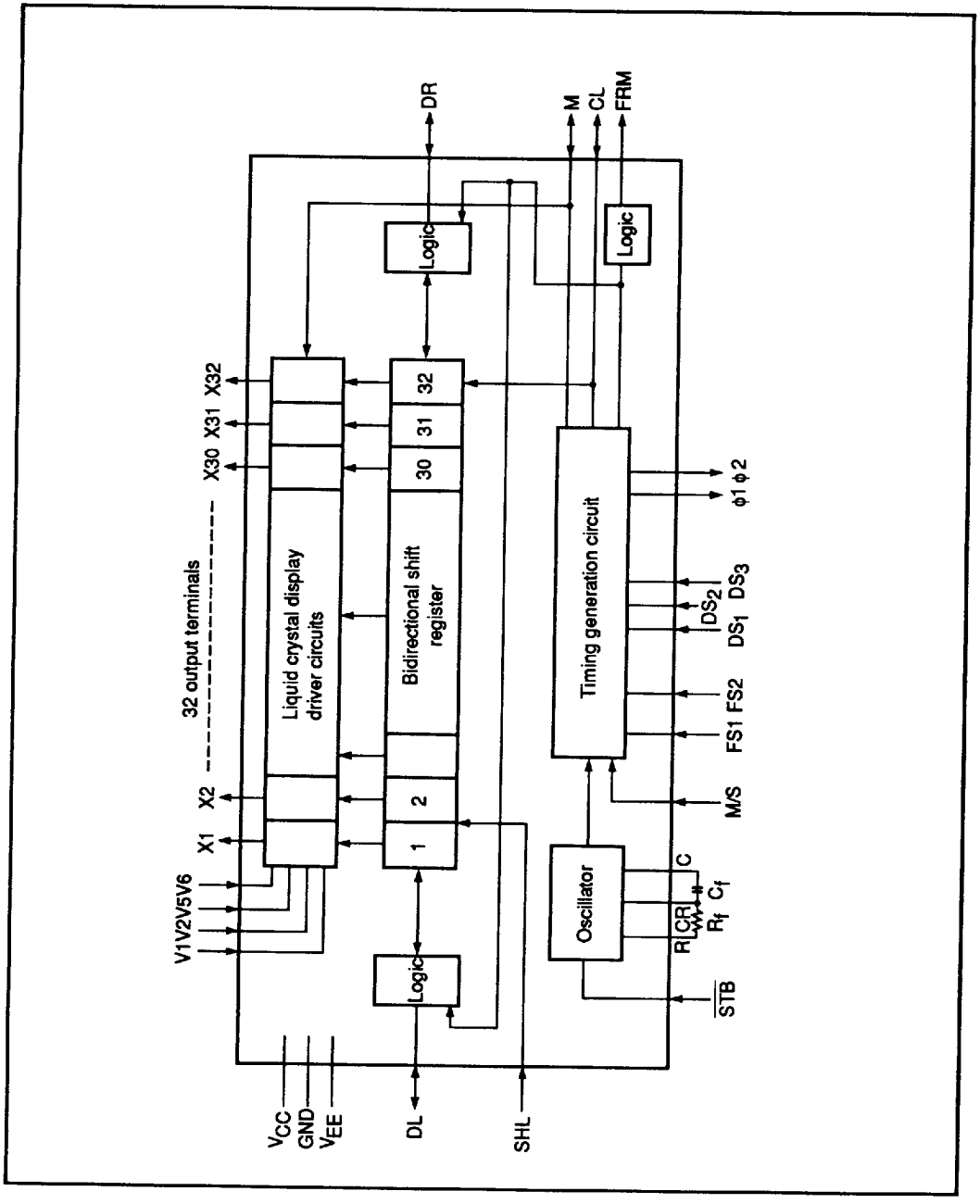
Pin Arrangement



(Top View)

Note: NCs show unused terminals.
Don't connect any lines to
them in using this LSI.

Block Diagram



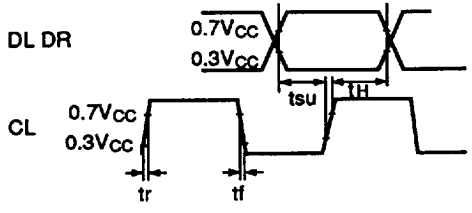
Electrical Characteristics

(Note 4)

(V_{CC} = +5 V ± 10%, GND = 0 V, V_{EE} = 0 to −5.5 V, Ta = −20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	0.7 × V_{CC}	—	V_{CC}	V		5
Input low voltage	V_{IL}	0	—	0.3 × V_{CC}	V		5
Output high voltage	V_{OH}	V_{CC} −0.4	—	—	V	I_{OH} = −400 µA	6
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 400 µA	6
Vi-Xj On resistance	R_{ON}	—	—	1000	Ω	V_{EE} = −5 V ± 10%, Load current ±15 µA	
Input leakage current (1)	I_{IL1}	−1	—	1	µA	V_{IN} = V_{CC} to GND	7
Input leakage current (2)	I_{IL2}	−5	—	5	µA	V_{IN} = V_{CC} to V_{EE}	8
Shift frequency	F_{SFT}	—	—	50	kHz	In slave mode	9
Oscillation frequency	f_{OSC}	300	430	560	kHz	Rf = 68 kΩ ± 2%, Cf = 10 pF ± 5%	10
External clock operating frequency	f_{CP}	50	—	560	kHz		11
External clock duty cycle	Duty	45	50	55	%		11
External clock rise time	t_{rCP}	—	—	50	ns		11
External clock fall time	t_{fCP}	—	—	50	ns		11
Dissipation power (Master)	P_{W1}	—	—	4.4	mW	CR oscillation, 430 kHz	12
Dissipation power (Slave)	P_{W2}	—	—	1.1	mW	Frame 70 kHz	13

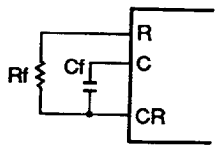
Notes:
4. Specified within this range unless otherwise noted.
5. Applied to CR, FS1, FS2, DS1 to DS3, M, SHL, M/S, CL, DR, DL, and $\overline{STB}$.
6. Applied to DL, DR, M, FRM, CL, φ1, and φ2.
7. Applied to input terminals CR, FS1, FS2, DS1 to DS3, SHL, M/S, and $\overline{STB}$ and I/O common terminals DL, DR, M, and CL at high impedance.
8. Applied to V1, V2, V5, and V6.
9. Shift operation timing.



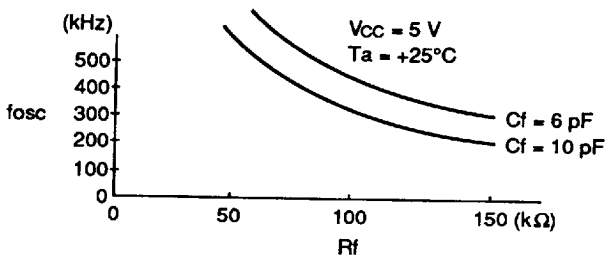
	Min	Typ	Max	Unit
tsu	5	–	–	µs
t_H	5	–	–	µs
tr	–	–	100	ns
tf	–	–	100	ns

Notes: 10. Relation between oscillation frequency and Rf, Cf.

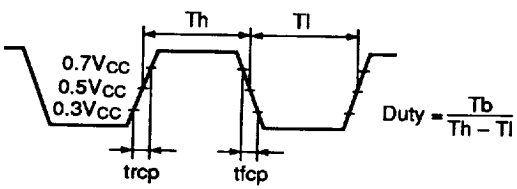
Connection

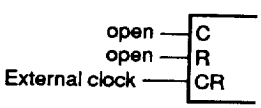


The values of Rf and Cf are typical values. The oscillation frequency varies with the mounting condition. Adjust oscillation frequency to a required value.



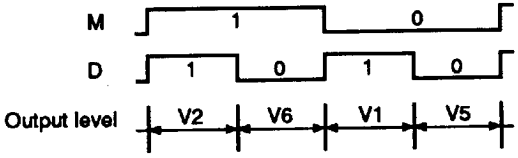
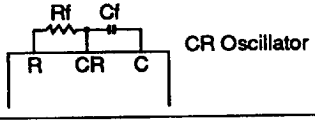
11.





12. Measured by V_{CC} terminal at output non-load of Rf = 68 kΩ ± 2% and Cf = 10 pF ± 5%, and 1/32 duty cycle in the master mode.
Input terminals are connected to V_{CC} or GND.
13. Measured by V_{CC} terminal at output non-load, 1/32 duty cycle, and frame frequency of 70 Hz in the slave mode.
Input terminals are connected to V_{CC} or GND.

Pin Description

Pin Name	Pin Number	I/O	Function
X1–X32	32	O	Liquid crystal display driver output. Relation among output level, M, and data (D) in shift register. 
CR, R, C	3		Oscillator.  CR Oscillator
M	1	I/O	Signal for converting liquid crystal display driver signal into AC. Master: Output terminal Slave: Input terminal
CL	1	I/O	Shift register shift clock. Master: Output terminal Slave: Input terminal
FRM	1	O	Frame signal, Display synchronous signal.
DS1–DS3	3	I	Display duty ratio select.

Display Duty Ratio	1/8	1/16	1/32	1/64	–	1/12	1/24	1/48
DS1	L	L	H	H	L	L	H	H
DS2	L	H	L	H	L	H	L	H
DS3	L	L	L	L	H	H	H	H

			Selects frequency.
FS1–FS2	2	I	The relation between the frame frequency f_{FRM} and the oscillation frequency fosc is as follows:

FS1	FS2	fosc(kHz)	f_{FRM}(Hz)	f_M(Hz)	f_{CP}(kHz)
L	L	107.5	70	35	53.8
H	L	107.5	70	35	53.8
L	H	215.0	70	35	107.5
H	H	430.0	70	35	215.0

f_{OSC}: Oscillation frequency
f_{FRM}: Frame frequency
f_M: M signal frequency
f_{CP}: Frequencies of $\phi 1$ and $\phi 2$

Pin Description (cont)

Pin Name	Pin Number	I/O	Function
$\overline{STB}$	1	I	Input terminal for testing. Connect this terminal to V_{CC}.
DL, DR	2	I/O	Data I/O terminals of bidirectional shift register.
SHL	1	I	Selects shift direction of bidirectional shift register. SHL: H — Shift Direction: DL → DR SHL: L — Shift Direction: DL ← DR
M/S	1	I	Selects Master/Slave. M/S = High: Master mode The oscillator and timing generation circuit operate to supply display timing signals to the display system. Each of I/O common terminals, DL, DR, M, and CL is in the output state. M/S = Low: Slave mode The timing generation circuit stop operating. The oscillator is not required. Connect terminal CR to V_{CC}. Open terminals C and R. One (determined by SHL) of DL and DR, and terminals M and CL are in the input state. Connect M, CL and one of DL and DR of the master to the respective terminals. Connect FS1, FS2, DS1, DS2, DS3, $\overline{STB}$ to V_{CC}. When display duty ratio is 1/8, 1/12, 1/16, 1/24, 1/32, one HD44105H is required. Use it in the master mode. When display duty ratio is 1/48, 1/64, two HD44105Hs are required. Use one in the master mode to drive common signals 1 to 32, and another in the slave mode to drive common signals 33 to 48(64).
$\phi1$, $\phi2$	2	O	Operating clock output terminals for HD44102CH. The frequencies of $\phi1$ and $\phi2$ are half of oscillation frequency.
V1, V2, V5, V6	4		Liquid crystal display driver level power supply. V1 and V2: Selected level V5 and V6: Non-selected level
V_{CC}, GND V_{EE}	3		Power supply. V_{CC} – GND: Power supply for internal logic V_{CC} – V_{EE}: Power supply for driver circuit logic

Block Functions

Oscillator

A CR oscillator attached to an oscillation resistor Rf and an oscillation capacitor Cf. The oscillation frequency v aries with the values of Rf and Cf and the mounting conditions. Refer to electrical characteristics (note 10) to make proper adjustment.

Timing Generation Circuit

This circuit divides the signals from the oscillator and generates display timing signals (M, CL, and FRM) and operating clock (ϕ1 and ϕ2) for HD44102CH according to the display duty ratio set by DS1 to DS3. In the slave mode, this block stops operating. It is meaningless to set FS1, FS2 and DS1 to DS3. However, connect them to V_{CC} to prevent floating current.

Bidirectional Shift Register

A 32-bit bidirectional shift register. The shift direction is determined by the SHL. The data input from DL or DR performs a shift operation at the rise of shift clock CL.

Liquid Crystal Display Driver Circuit

Each of 32 driver circuits is a multiplex circuit composed of four CMOS switches. The combination of the data from the shift register with the M signal allows one of the four liquid crystal display driver levels V1, V2, V5, and V6 to be transferred to the output terminals.

Connection between HD44105H and HD44102CH